REMARKS

Claims 1-4, 6-10, and 12-26 are pending.

This case was on appeal. The Final Office Action of July 28, 2005 (Second Final Office Action) has reopened prosecution and a new grounds of rejection.

Appreciation is expressed for the allowance of claim 15.

Appreciation is expressed for the examiner interview with Examiner Mehdi Namazi with Applicants' Attorney David G. Dolezal on September 28, 2005. During the interview, the claims were discussed.

Claims 1-4, 6-10, 12-14, and 16-26 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Okuno, U.S. Patent No. 6,105,114 (Okuno) in view of Morgan, U.S. Patent No. 6,083,271 (Morgan). These rejections are traversed for at least the reasons set forth below.

Independent Claim 1

a. The prior art does not teach non volatile memory cells

Okuno and Morgan, either alone or in combination, do not disclose or suggest "wherein the array of addressable storage elements comprises a plurality of nonvolatile memory cells," all as recited in independent claim 1.

Claim 1 was rejected in Section 2 of the Second Final Office Action. Section 2 states that Okuno fails to teach a storage with a plurality of nonvolatile memory cells.

Section 2 of the Second Final Office Action states that Morgan discloses a RAM which does not permanently store information. However, the Second Final Office Action states that "to make a RAM memory non-volatile, it is known to connect a battery to RAM device (col. 6, lines 4-6)."

Applicants respectfully submit that Morgan does not teach non volatile memory cells. As stated above, Morgan teaches that a RAM is a volatile memory that does not retain information

once power is removed. Accordingly, a RAM has volatile memory cells, and not non volatile memory cells. Even if Morgan suggests that connecting a battery to the RAM provides a memory that is non-volatile, it does not change the volatile characteristics of the memory cells of the memory array. If power (e.g. battery power) is removed from the cells, any data stored would be lost. Since claim 1 cites "non volatile memory cells" and not a "non volatile memory," such characteristics are not taught nor suggested by Morgan.

b. No motivation to combine Okuno and Morgan

In regards to the motivation to combine Okuno with Morgan, the Second Final Office Action states:

> "it would have been obvious to one having ordinary skill ... to incorporate the method of connecting a battery to a RAM device to make a non-volatile memory as taught by Morgan in corresponding to the storage device of Okuno. The modification would be obvious because of one ... would be motivated to connect a battery to a RAM device in order to make the information stored in the battery-backed RAM device non-volatile (col. 6, lines 5-7)."

Applicants respectfully submit that making information stored in RAM non volatile is not a proper motivation under 35 USC 103(a) for one of skill in the art to add a battery backup system as taught by Morgan to the memory circuitry of Okuno. Nowhere in Okuno does it suggest that it would be desirable to non volatilely store the information in the memory array of Okuno.

Okuno teaches a transposition circuit for implementing a transforming coding technique using a two-dimensional discrete cosine transform for coding image data such as MPEG data. Okuno, column 1, lines 8-25. Okuno implements a transposition memory circuit 1 for performing these operations. Okuno, column 7, lines 31-47. The circuit of Okuno is used for decoding multiple blocks of image data with a read and write operation being performed to each

cell of array 2 for each block of data being processed. Okuno, column 7, line 31- column 8, line 36.

Nowhere in Okuno does it require circuit 1 of Okuno to be able to store data when the power is off, nor is there any suggestion of it being desirable to save the data in memory array 2. In fact, memory array 2 is not utilized to store data for any substantial period of time. Okuno appears to teach that data is only "stored" in memory array 2 during a cycling of the addresses as provided by counter 20 to perform the transposition operations. See Okuno, column 8, lines 9-13 and in general column 9, line 31 – column 10, line 34. Since circuit 1 is part of a coding system for image data, there is no need to store data in array 2 when circuit 1 does not have power in that circuit 1 would not be used to encode data when there is no power. Because there is no need to store data in array 2 of Okuno (other than for a short period of time during a transposition operation), there is no reason for one of skill in the art to modify Okuno to include the extra circuitry and complexity of a battery backed system as taught by Morgan.

Furthermore, Okuno teaches away from adding the additional circuitry of a battery backed system as taught by Morgan.

Okuno teaches (at many locations in its specification) that it is highly desirable to reduce circuit size and reduce power consumption. Okuno, column 1, lines 11-14; column 3, lines 57-64; column 4, lines 5-9 and lines 36-40; column 5, lines 12-14, lines 18-21, and lines 40-43; column 6, lines 8-10, lines 21-23, and lines 56-58; and column 11, lines 31-36. See as an example the Summary Of The Invention section of Okuno (column 4, lines 5-9) where it states "One object of the present invention is to provide a two-dimensional array transposition circuit having a reduced amount of memory for reducing circuit scale and power consumption."

Morgan on the other hand teaches that adding a battery back up for a RAM would require additional circuitry. For example, Column 6, lines 7-10 state that "An IC that incorporates the battery-backed RAM device requires two power domains one domain for its regular power DC source and another power domain for the battery." See also Column 6, lines 46-50 where it states that "cache memory 5 has a first power and ground domain for the D.C. power source while the circuit is in its nominal state and a second power and ground domain for the battery when the circuit is not powered on." In such a system, at least one or more I/O cells will be needed to provide both power and ground sources to the cache memory. Morgan, Column 7, lines 59-61. Furthermore, such a system will require multiple pins for the multiple power and ground domains (Column 9, lines 3-5) as well as multiple busses (see Column 9, lines 26-33). See several examples in Columns 9-11 of Morgan of additional circuitry required for the battery back up system as taught by Morgan.

In addition to the extra circuitry required for a battery back up system, the battery itself will take up additional space and require charging, monitoring, voltage regulation, and power management circuitry and software. See Column 8, lines 9-27 of Morgan. Not only will the extra circuitry increase the size of the system of Okuno, it will also increase the power usage in operating this circuitry and performing software processing for the power management circuitry.

Furthermore, when DC power is removed, Morgan teaches the cache 5 will be consuming battery power when the circuit is not in operation. Morgan, Column 8, lines 15-18. Accordingly, providing a battery back up to the memory circuitry of Okuno would cause the memory circuitry of Okuno to consume more power.

Thus, one of ordinary skill in the art would not be motivated to modify the memory array 2 of Okuno to provide a battery back up as taught by Morgan in that such a modification of

would defeat the stated objectives of Okuno of reduced circuit size and reduced power consumption. Not only would implementing a battery back up as taught by Morgan increase the size of memory array 2 of Okuno due to the additional power domain circuitry, but it would also require the system of Okuno to include extra circuitry for charging, monitoring, voltage regulation, and power management circuitry and software as well. In addition, extra space would be needed for the battery itself. In addition, the memory array of Okuno would be consuming additional power when the system is not in operation. Since nowhere in Okuno does it teach or even suggest the desirability of having a non volatile memory, one of skill in the art would not be motivated to add the extra circuitry and increased power consumption of a battery backed system to Okuno, especially since Okuno teaches the desirability of less circuitry, less space, and reduced power consumption. Accordingly, claim 1 is allowable over Okuno and Morgan.

Independent Claim 6

For reasons similar to those stated above with respect to independent claim 1, Okuno and Morgan, either alone or in combination, do not disclose or suggest wherein the array of storage elements comprises a plurality of nonvolatile memory cells," all as recited in independent claim 6.

In addition, the Second Final Office Action has not set forth a proper motivation to combine the teachings of Okuno and Morgan in the rejection of claim 6. See the discussion above with respect to claim 1. Accordingly, claim 6 is allowable over Okuno and Morgan.

Dependent claim 12

Okuno and Morgan, either alone or in combination, do not disclose or suggest wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell, all as recited by claim 12.

Neither Okuno nor Morgan disclose a floating gate-type memory cell.

Regarding dependent claim 12, Section 2 of the Second Final Office Action states that "Okuno teaches wherein each of the plurality of nonvolatile memory cells comprises a floating gate-type cell (it is inherent to use floating gate to detect the threshold voltage states of the cell transistor)."

Applicants respectfully submit that Section 2 is incorrect with respect to its discussion of claim 12. For example, Okuno does not teach non volatile memory cells.

Also, Applicants respectfully submit that the statement "it is inherent to use floating gate to detect threshold states of the cell transistor," is also incorrect.

To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference. MPEP Section 2112, Subsection IV. Applicants respectfully submit that a floating gate-type cell is not necessarily present in memory array 2 of Okuno.

Accordingly, if this rejection is to be maintained, Applicants respectfully request that the Examiner provide a basis in fact and/or technical reasoning to reasonably support the determination that a floating gate-type cell is necessarily present in the memory array of Okuno. See MPEP 2112, Subsection IV. Accordingly, claim 12 is allowable over Okuno and Morgan.

Claim 14

For reasons similar to those stated above with respect to independent claim 1, Okuno and Morgan either alone or in combination, do not disclose or suggest an array of nonvolatile memory cells, all as recited in independent claim 14.

In addition, the Second Final Office Action has not set forth a proper motivation to combine the teachings of Okuno and Morgan in the rejection of claim 14. See the discussion above with respect to claim 1. Accordingly claim 14 is allowable over Okuno and Morgan.

Claim 16

For reasons similar to those stated above with respect to independent claim 1, Okuno and Morgan either alone or in combination, do not disclose or suggest a plurality of nonvolatile memory cells, all as recited in independent claim 16.

In addition, the Second Final Office Action has not set forth a proper motivation to combine the teachings of Okuno and Morgan in the rejection of claim 16. See the discussion above with respect to claim 1. Accordingly claim 16 is allowable over Okuno and Morgan.

Claim 22

For reasons similar to those stated above with respect to independent claim 1, Okuno and Morgan either alone or in combination, do not disclose or suggest an array of nonvolatile memory cells, all as recited in independent claim 22.

In addition, the Second Final Office Action has not set forth a proper motivation to combine the teachings of Okuno and Morgan in the rejection of claim 22. See the discussion above with respect to claim 1. Accordingly claim 22 is allowable over Okuno and Morgan.

Claim 25

For reasons similar to those stated above with respect to independent claim 1, Okuno and Morgan either alone or in combination, do not disclose or suggest an array of nonvolatile memory cells, all as recited in independent claim 25.

In addition, the Second Final Office Action has not set forth a proper motivation to combine the teachings of Okuno and Morgan in the rejection of claim 25. See the discussion above with respect to claim 1. Accordingly claim 25 is allowable over Okuno and Morgan.

Other Dependent Claims

Each dependent claim depends from an independent claim and is allowable for at least this reason.

The application is believed to be in condition for allowance and notice of such is respectfully requested. If there is any remaining issues, the Examiner is respectfully requested to telephone the undersigned.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079.

Respectfully submitted,

By: _____

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